ANALOG DEVICES

AN-742
APPLICATION NOTE

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Frequency Domain Response of Switched-Capacitor ADCs

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INTRODUCTION

Knowing the frequency response of analog-to-digital converters (ADCs) with a switched-capacitor front end is an important first step in understanding how to design an interface to these types of pipeline ADCs. The characteristic input impedance that the ADC exhibits must be determined before designing any interface, regardless of whether it is active, passive, dc-open, or ac-coupled. The interface must also be connected to get the best response and performance from the ADC.

This application note develops a method using measurements made with a network analyzer in order to provide a better understanding of the input response over a wide frequency range and allows users to design a more effective interface to an ADC with switched-capacitor inputs. All measurements and model calculations were made using the AD9236 in a 32-lead chip scale package (CSP).

The ADC's sample-and-hold amplifier circuit (SHA) is mainly comprised of an input switch, an input sampling capacitor, a sampling switch, and an amplifier. As Figure 1 shows, the input switch interfaces the driver circuit with the input capacitor. When the input switch is on (track mode), the driver circuit drives the input capacitor. The input is sampled (captured) on the input capacitor at the end of this mode. When the input switch is off (hold mode), the driver is isolated from the input capacitor. The track mode period and the hold mode period of the ADC are approximately equal.

The interface problem with a switched capacitor front end ADC is seen as two fold—the frequency domain response, which this application note will present, and time domain response. The first, is that the input impedance of the ADC during the track mode of the SHA is different from the input impedance of the ADC during the hold mode of the SHA. This makes it difficult to accurately impedance match the ADC input with the driver circuit. But, since the ADC looks at the input signal only during the track mode of the SHA, the input impedance should be matched for this mode. The frequency dependence of the input impedance is governed mainly by the sampling capacitor and any parasitic capacitance in the signal path. For accurate impedance matching, it is helpful to have an idea of the frequency dependence of the input impedance. The measurement results obtained from the AD9236 explain the behavior of the input impedance for various input frequencies. The Example section of this note will then show a way to determine an input interface with the ADC during the track mode.

The second problem lies in the time domain where the switched capacitor front end presents "kickback" into the driver circuit. This problem occurs when the ADC switches from one mode to the other, charging the input capacitors from the previous sample to the current sample. Hence, the current glitch occurring at the input of the ADC is dependent on three factors—the difference between the previous and the current samples, the

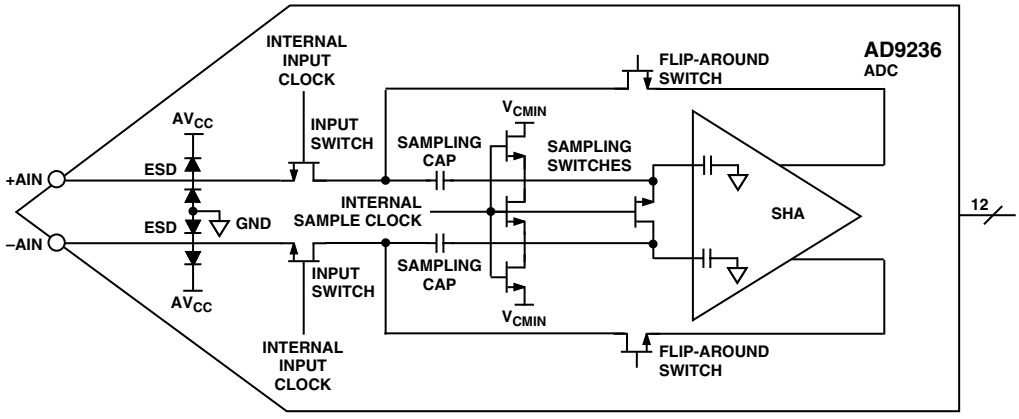

Figure 1. AD9236 Input Front End Model

value of the input sampling capacitor, and the sum of all resistances in the signal path (this is comprised of the on-resistance of the switches in the signal path and any series resistance in the signal path).

If the nonlinear portion of the current glitch corrupts the input sample when the driver has a linear response, the signal will distort. Therefore, it is crucial to select a driver capable of settling the current glitch within a half-clock cycle to preserve the ADC's performance.

METHOD

To understand its frequency response, we accurately measured the front end of an AD9236 using a network analyzer. An AD9236 evaluation board was cut in half to keep the input traces short and to minimize as many board parasitics as possible. The evaluation board was biased at nominal supply voltages and clocked at 1 MSPS. Figure 2a shows the timing setup used to ensure that the network analyzer sampled during the track mode of the ADC. The duty cycle of the ADC clock was set to 90% (not shown Figures 2a or 2b) to provide leeway for the ADC's input settling and the network analyzer delays. The same setup was used to take measurements during the hold mode, except that the ADC clock was inverted, as shown in Figure 2b.

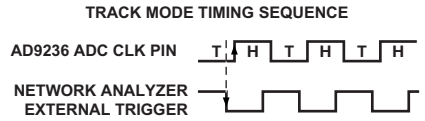

Figure 2a. Timing Diagram Setup–Track Mode

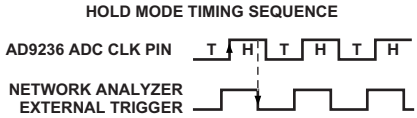

Figure 2b. Timing Diagram Setup–Hold Mode

The measurement setup is shown in Figure 3. The network analyzer was configured to capture 1601 points over a 300 kHz to 1 GHz frequency range. A two-channel pulse generator with matched cables was used to strobe the evaluation board and external trigger of the network analyzer. Power supplies were applied to properly bias the front end and provide a common-mode voltage of +1.5 V to each analog input. Timing to meet the requirements presented in Figure 2 was verified by a digital oscilloscope. Measurements were made on the evaluation board, and also on an error board, which is a portion of the evaluation board containing the same trace parasitics seen by the ac coupling capacitor, and two common-mode resistor dividers that develop the common-mode voltage on the analog inputs. The error board data is used to de-embed the errors caused from these sources, allowing the ADC input structure to be measured independently (See Equation 1).

Evaluation Board (parasitics + AD9236) - Error Board (parasitics) = Evaluation Board (AD9236) (1)

MEASUREMENTS

The measurements taken are in single-ended form. Due to the network analyzer's limited capabilities however, a popular method of converting these measurements from single-ended to differential was used. The following equation converts a single-ended measurement to differential by using the LogMag scattering parameters (S-parameters) S11, S12, S21, and S22 from the network analyzer.

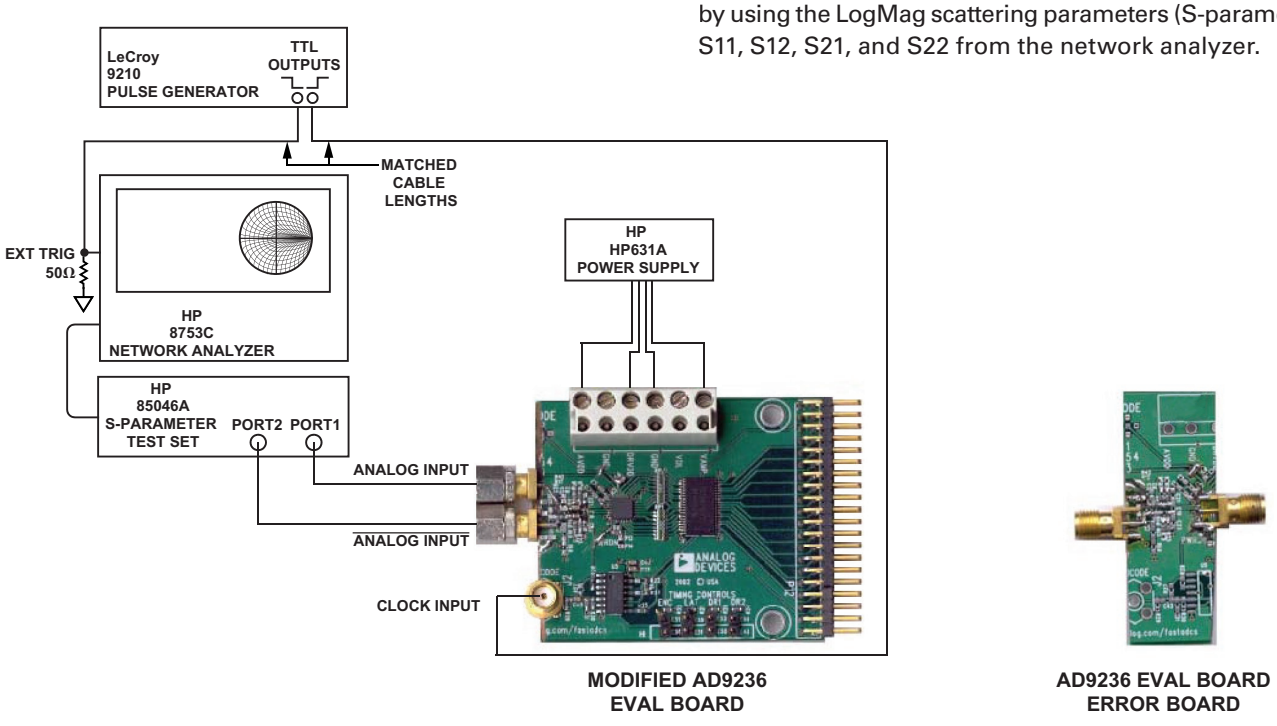

Figure 3. Network Analyzer Measurement Setup

$$\Gamma_S = \frac{(2\times S11-S21)(1-S22-S12)+(1-S11-S21)(1+S22-2\times S12)}{(2-S21)(1-S22-S12)+(1-S11-S21)(1+S22)} \quad (2)$$

A differential impedance, Z_{DIFF}, can be derived by taking Equation 2 a step further, as shown in Equation 3. This produces the equivalent parallel real and imaginary impedance (Z_{DIFF}) circuit from the series type measurement.

$$Z_{DIFF} = 50 \times [(1+\Gamma)/(1-\Gamma)] = R \pm jX \quad (3)$$

Using the Advanced Design System© (ADS) software simulation package from Agilent Technologies, data was exported from the network analyzer, converted to differential, and the common-mode component error was subtracted out (See Figure 5).

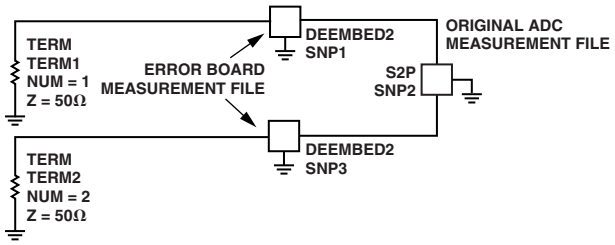

Figure 4. ADS Configuration Setup

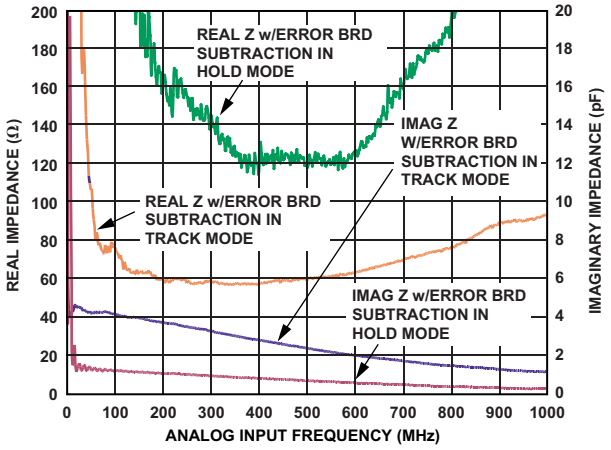

Figure 5. Differential Input Impedance vs. Analog Input Frequency

RESULTS

The result of these computations shows real and imaginary components in both track-and-hold modes. The values that represent the real part in ohms are located on the left side of Figure 5. The values that represent the imaginary or capacitive part in pF are located on the right side of Figure 5.

In track mode (at low frequencies), the real part looks like a very high impedance, settling to roughly 60 Ω at 200 MHz. Referring back to the ADC input model of Figure 1, the input impedance is approximately equal to the resistive equivalent of the series-parallel combination of transistors in the track mode. The imaginary part starts at 4 pF at 200 MHz, rolling off to 1 pF at 1 GHz. These values are to be expected, because the input stage of the ADC during the track mode is the sum of the series-parallel combination of the transistors' parasitic capacitance. In hold mode, the real part of the impedance is much higher, dropping to roughly 120 Ω at 500 MHz, then increasing as it approaches 1 GHz. The real impedance in the hold mode was expected to be much higher (>10 kΩ) at all frequencies, so further investigation is necessary to explain the measurement results. It is thought that the analog input ESD structures cause part of the high-frequency measurement error. The imaginary part, however, quickly falls to 1 pF or less throughout the entire measurement range, as was expected for the ESD and package parasitics. This is due to the input structure looking essentially like an open circuit (as shown in the ADC input model of Figure 1).

Figure 6 shows an expanded view of Figure 5 that depicts the usable frequency range of the ADC.[1]

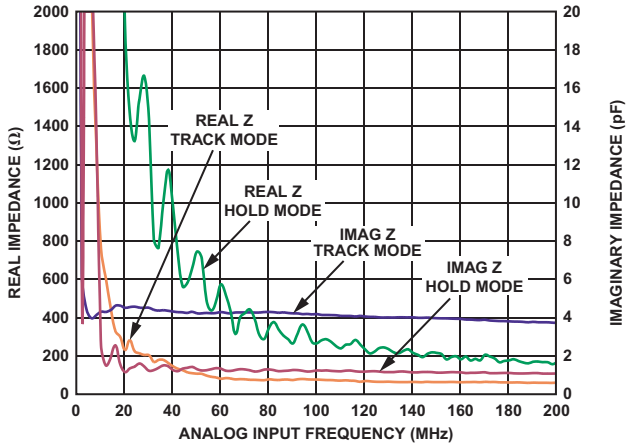

Figure 6. Differential Input Impedance vs. Analog Input Frequency (Expanded)

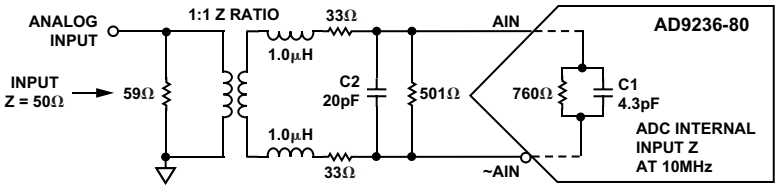

Figure 7. Differential Termination Example

EXAMPLE

Now let us look at an example of how to interface with the AD9236 using a transformer coupled input based on the measured results. With an analog input frequency at 10 MHz, the AD9236 looks like a 760 Ω differential resistor and 4.3 pF capacitor during the track mode[1]. If the input impedance is designed to 50 Ω then one implementation could be represented as shown in Figure 7.

Other advantages gained from using this circuit topology when designing interface circuits for switch-capacitor ADCs include cancellation of even-order distortion products by having a matched differential input termination, as well as high common-mode rejection from switching transients (note the two 33 Ω and 501 Ω resistors). Also a capacitor value could be determined based on the amount of bandwidth wanted for your particular application. For this example a 20 pF was chosen for a filter cutoff of 120 MHz.

The key is to make the input look as "real" as possible to achieve a good impedance match to the preceding components as this example shows. Since the input is capacitively dominated, the goal here is to find a matching inductive term in order to cancel the imaginary impedance. Let us now look at the math involved in order to complete this operation using complex terms.

$$X_{C1} = \frac{1}{2\pi 10M4.3p} = -j3.7k\Omega,\ X_{C2} = \frac{1}{2\pi 10M20p} = -j796\Omega$$

(760–j0) || (0–3.7 k) = (729.23–j149.78) Ω
(729.23–j149.78) || (501+j0) = (299.95–j24.48) Ω
(299.95–j24.48) || (0–j796) = (249.04–j114.79) Ω
Set X_L = 114.8 Ω and solve for L at 10 MHz, this equals 1.83 µH.

Now that L has been found, divide it equally and place it in series with the 33 Ω resistors on the secondary of the transformer as shown in Figure 7.

(249.04–j114.8) + (66+j114.8) = 315.04 Ω

Add all of the components together to find the resulting impedance seen at the secondary of the transformer. Remember, we added in the L to have the input look mostly real.

The transformer has a 1:1 impedance ratio therefore, 315 Ω is the impedance seen at the primary of the transformer in parallel with the 59 Ω resistor. These two resistors in parallel further yield the 50 Ω termination, 315 || 59 = 50 Ω.

With the ADC input S-parameters at hand, a better expectation of the preceding filter or amplifier's load termination can be defined as this example shows. This allows the designer to minimize the load mismatches, which result in gain and rolloff variations in the passband. Ultimately, it is these types of variations that can cause noise and distortion degrading the ADC's expected performance. An exaggerated example of a particular filter response is shown in Figure 8. Note that the frequency response of the filter changes as the load termination changes. This simple illustration gives the designer a feel for what to expect when designing the ADC interface without further compensation.

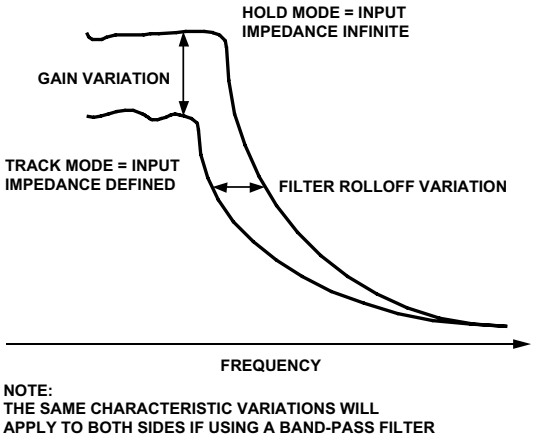

Figure 8. Illustrated Filter Response Due to Load Variation

CONCLUSION

This application note shows the typical[2] impedance values that can be expected from a switched-capacitor ADC, which is useful for designing a front end interface. The data presented here is specific to the AD9236 in a CSP package, describing the general behavior of this switched-capacitor ADC family, including the AD9229, AD9235, AD9238[3], AD9245, and AD9248. The designer should keep in mind that the results presented also incorporate the CSP package style parasitics. Using any of these devices in a different package style will yield slightly different results. Further investigation will be completed on other switched-capacitor ADC families and can be found at www.analog.com.

REFERENCES

1. AD9236 Data Sheet, Analog Devices, Inc., Norwood, MA, www.analog.com.
2. Advanced Design System (ADS) Software 2003C, Agilent Technologies, Santa Clara, CA, www.agilent.com.
3. ENA Series RF Network Analyzers User's Guide, Agilent Technologies, Santa Clara, CA, www.agilent.com.
4. HP 8753C Network Analyzer Reference, Agilent Technologies, Santa Clara, CA, www.agilent.com.
5. Kester, Walt, ed. *Analog-to-Digital Conversion*, Analog Devices, Inc., 2004, ISBN 0-916550.

[1]For further information, go to www.analog.com/AN-742Worksheet. Here, the AD9236 Analog Input S-Parameter Data (real and imaginary component values) can be referred to in a tabular format against frequency.
[2]Typical performance entails no power supply variation and temperature at 25°C only.
[3]The AD9238 is only available in a quad flat pack (QFP) style.

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